REMARKS

Applicants appreciate the allowance of Claims 51-57. The non-elected claims have been canceled without prejudice to pursing them in a related divisional application.

Applicants will now address each of the Examiner's remaining objections and rejections in the order in which they appear in the Office Action.

Drawings

The Examiner objects to Figure 15 and is requiring it be designated by the legend -- Prior Art -- . Applicants have now done so and request that this objection be withdrawn.

Claim Rejections - 35 USC §103

In the Office Action, the Examiner rejects Claims 1, 3, 5, 7, 11, 12, 13, 16, 23, 25, 27, 32, 34, 36, 43, 47, 65-80 under 35 USC §103 as being unpatentable over Takahara et al. in view of Kimura et al.

While Applicants respectfully traverse this rejection, in order to advance the prosecution of this application, Applicants have amended independent Claims 1, 3, 5, 7, 65 and 72 to include the feature of a time division gray-scale data signal generating circuit comprising a plurality of thin film transistors over a substrate for dividing one frame period into a plurality of sub-frame periods. As the Examiner has stated in the Office Action that none of the references disclose nor can be combined to yield this feature, these independent claims and those claims dependent thereon are patentable over the cited references. Accordingly, it is requested that this rejection be withdrawn.

Information Disclosure Statement

Applicant is submitting an IDS herewith. It is respectfully requested that this IDS be entered and considered before any further action is entered in this application.

Please charge our deposit account 50/1039 for any fee due for this IDS.

Conclusion

It is respectfully submitted that the present application is in a condition for allowance and should be allowed.

If any fee is due for this amendment, please charge our deposit account 50/1039.

Favorable reconsideration is earnestly solicited.

Respectfully submitted,

Date: May 13, 2004

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Registration No. 34,225

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